

REMARKS

Claims 1-22 were originally filed in the present application.

Claims 1-22 are pending in the present application.

Claims 1-22 were rejected in the June 28, 2005, Office Action.

No claims have been allowed.

Claims 1-4, 10-13 and 19-22 are amended herein

Claims 1-22 remain in the present application.

Reconsideration of the claims is respectfully requested.

In Section 1 of the June 28, 2005 Office Action, the Examiner objected to the disclosure for informalities on pages 35 and 36. In response, the Applicants have amended the paragraph bridging pages 35 and 36 to correct the informalities. The Applicants respectfully submit that no new matter is added in the replacement paragraph.

The Examiner also objected to references on page 40 of the disclosure to Appendices A-E. In the Applicants' copy of the application as filed, Appendices A-E appear as pages 45-49. If those pages are missing from the Examiner's copy of the application, the Applicants will provide the missing pages in a subsequent reply. In reviewing the Appendices, the Applicants noted that Appendix C, on page 47, was filed without a label and herewith submit a replacement page showing Appendix C properly labeled. The Applicants respectfully submit that no new matter is thereby added and request withdrawal of the objections to the specification.

In Section 3 of the June 28, 2005 Office Action, the Examiner objected to Claims 1-22 for identifying output signals from input detectors of the present invention as “[+1,+1]” and “[-1,-1]” and suggested identifying the output signals as “(+1,+1)” and “(-1,-1)”, instead. The Applicants note that usage of square brackets in the claims is consistent with their usage in the specification and respectfully decline to make the suggested amendment to the claims. The Applicants respectfully request withdrawal of the objection to the claims, or citation by the Examiner of a specific rule in 37 C.F.R. or in the MPEP in support of the objection.

In Section 4 of the June 28, 2005 Office Action, the Examiner rejected Claims 1-22 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicants regard as the invention. The Examiner asserted that the variable identifiers S, M and N are undefined in independent Claims 1, 10 and 19. The Applicants respectfully traverse the rejection.

The Applicants draw the Examiner’s attention to the preamble of Claim 1, which recites:

1. A demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M=2^N$, said demodulator comprising:...

The Applicant respectfully asserts that the identifiers S, M and N are, in fact, variable names that are defined in the preamble. The variable S is the number of possible orthogonal modulation codes in a set of codes demodulated by the demodulator being claimed. The variable N is the number of bits in a data symbol represented by one of the orthogonal modulation codes. The variable M is the number

of binary bits in the data symbol and is specified as equal to 2^N . Accordingly, the Applicants respectfully request that the rejection of Claims 1-22 under §112, second paragraph, be withdrawn.

In Sections 6 and 7 of the June 28, 2005 Office Action, the Examiner rejected Claims 1-22 under the judicially created doctrine of double patenting over Claims 1-22 of copending Application No. 10/038,869. The Examiner asserted that the first two of the four two-bit input detectors of the present application perform the same function as the two single-bit input detectors of the copending application. In response, the Applicants have amended Claims 1-4, 10-13 and 19-22 in order to more particularly point out and distinctly claim the Applicants' invention.

The single-bit input detectors recited in the claims of the copending application receive the bits of a binary input data in sequence—Bit 0, Bit 1, Bit 2, Bit3, etc. In contrast, the two-bit input detectors recited in the amended claims of the present application receive the bits in sequential, non-overlapping pairs—Bit 0 and Bit 1, followed by Bit 2 and Bit 3, etc. In order to perform the same function as the two single-bit input detectors of the copending application, the first two of the four two-bit input detectors of the present application would have to process the bits in sequential, overlapping pairs—Bit 0 and Bit 1, followed by Bit 1 and Bit 2, followed by Bit 2 and Bit 3, etc. As amended, the claims of the present invention do not recite input detectors that process the bits in such a sequence.

As such, the Applicants respectfully request that the rejection of Claims 1-22 under the judicially created doctrine of double patenting over Claims 1-22 of copending Application No. 10/038,869 be withdrawn.

The Applicants thank the Examiner for the indication that Claims 1-22 would be allowable if rewritten to overcome the objections, the rejection under 35 U.S.C. §112, second paragraph, and the rejection under the judicially created doctrine of double patenting over Claims 1-22 of copending Application No. 10/038,869. The Applicants respectfully submit that the objections and rejections have been traversed and the claims are now in condition for allowance.

SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *jmockler@davismunck.com*.

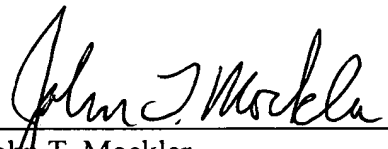
The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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PATENT

APPENDIX C - Code Mask 01 Table

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